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Low power DAC sub-system for Digital Beam Forming chip

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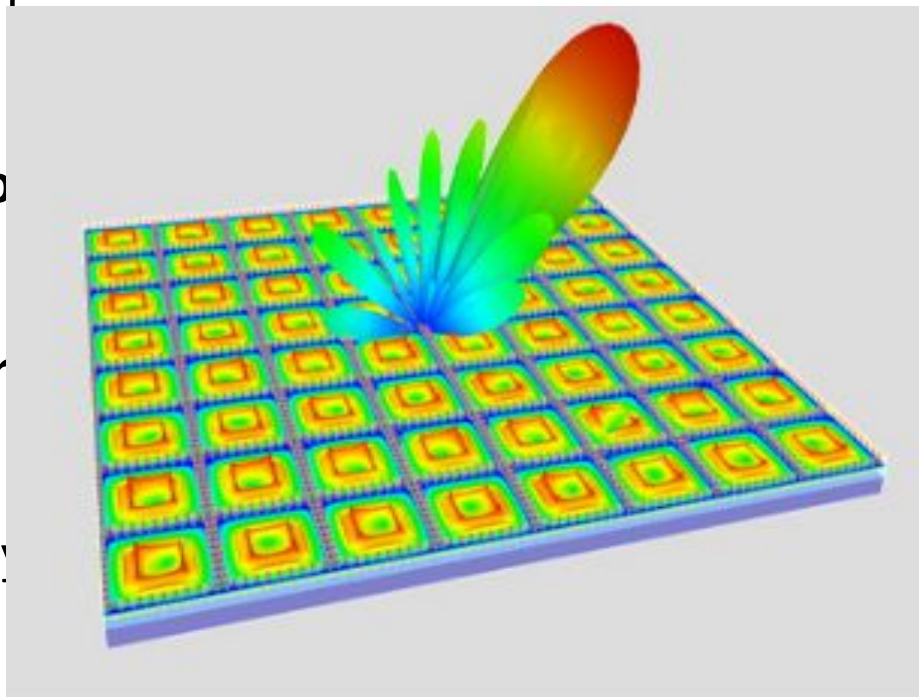
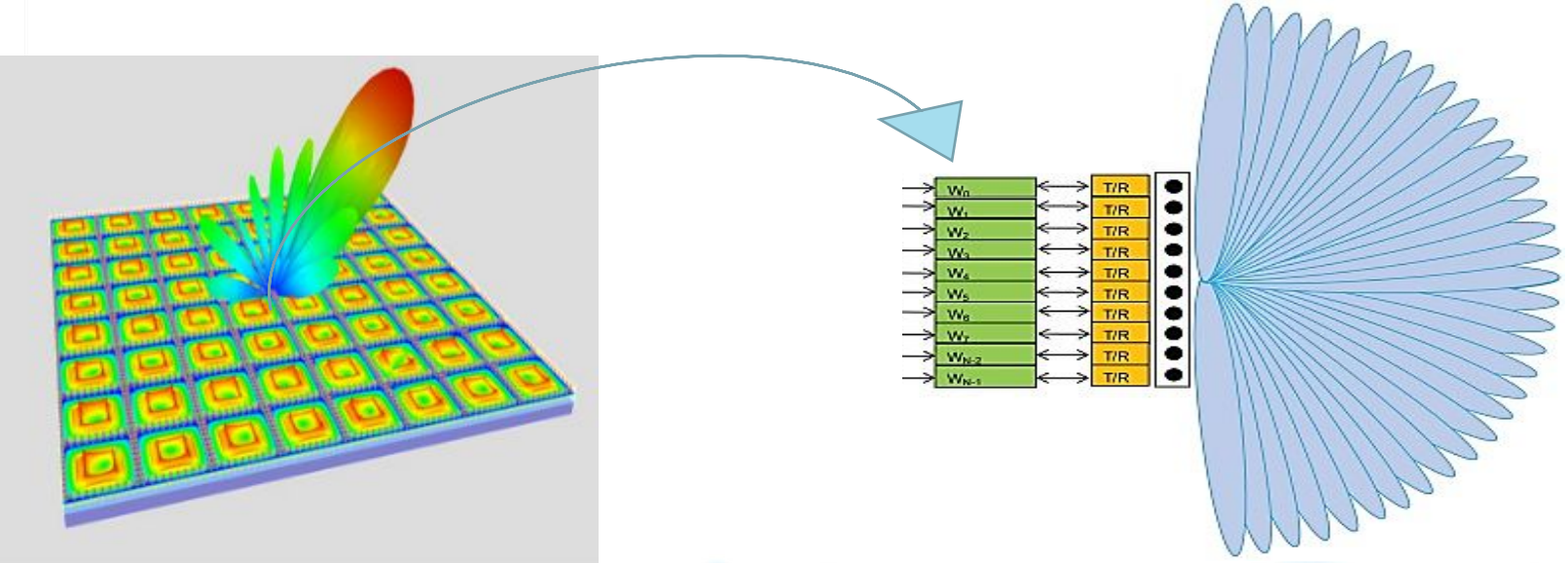
Motivation

- Cutting edge satellite, terrestrial and 5G wideband communication use Digital Beam forming.
- There are hundreds of RF-Transmitter in Digital Beam forming
- These RF-chains need **highly efficient DAC (Digital to Analog Convertor)**
- **High number of DACs per antenna -** makes the **power consumption** a critical parameter DAC
- Process technology and standard cell optimizations will only shave off a small percentage of power
- We need a **major architectural innovation** to reduce the power consumption

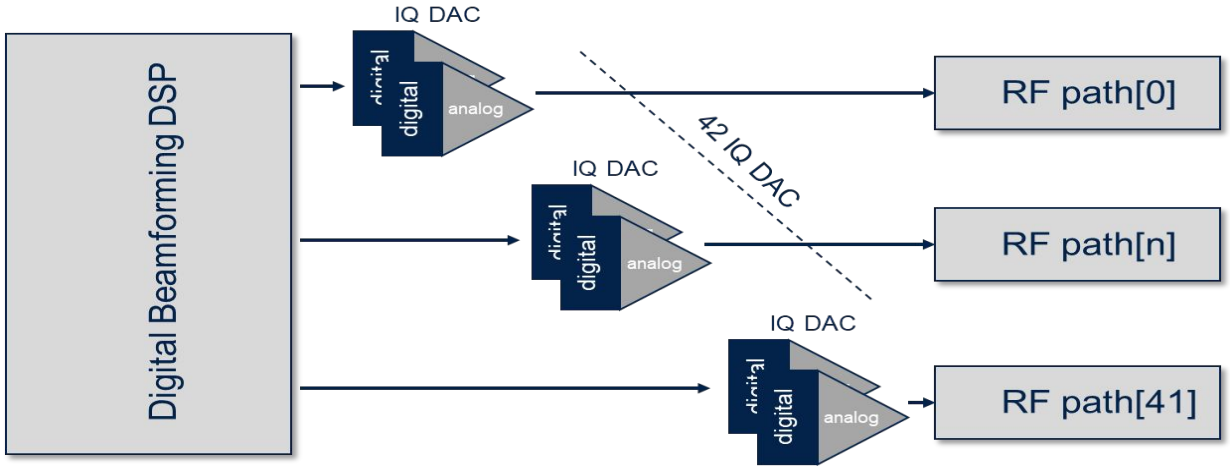


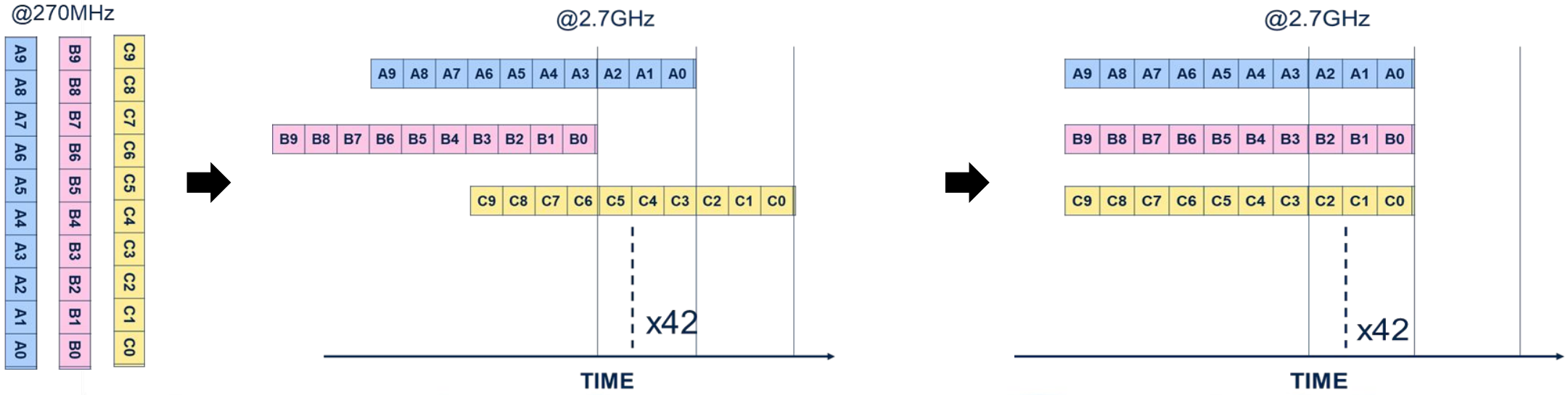
Digital Beam Forming (DBF)

- In digital beam forming, multiple RF chain feeding the antenna array
- It provide full control of phase, gain and signal shape for each RF chain
- Superimposed emission of multiple channels produces multiple simultaneous beams
- DBF is extremely flexible and can provide wide coverage and high resolution at the same time
- DBF requires a group delay calibration of multiple high frequency data channels that drive HF-DACs



Digital Beam Forming

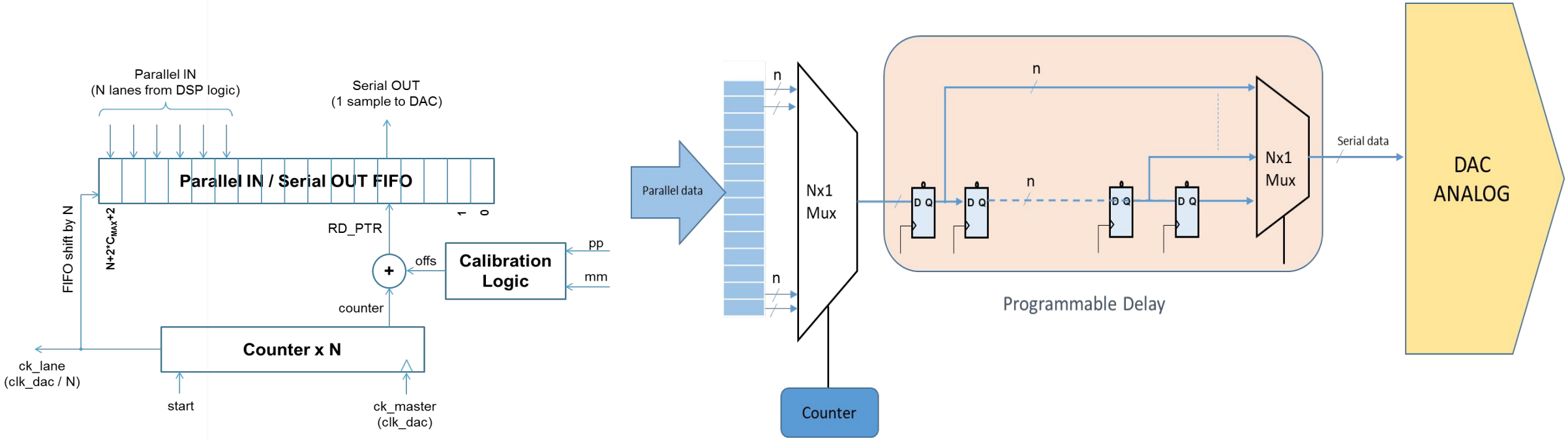




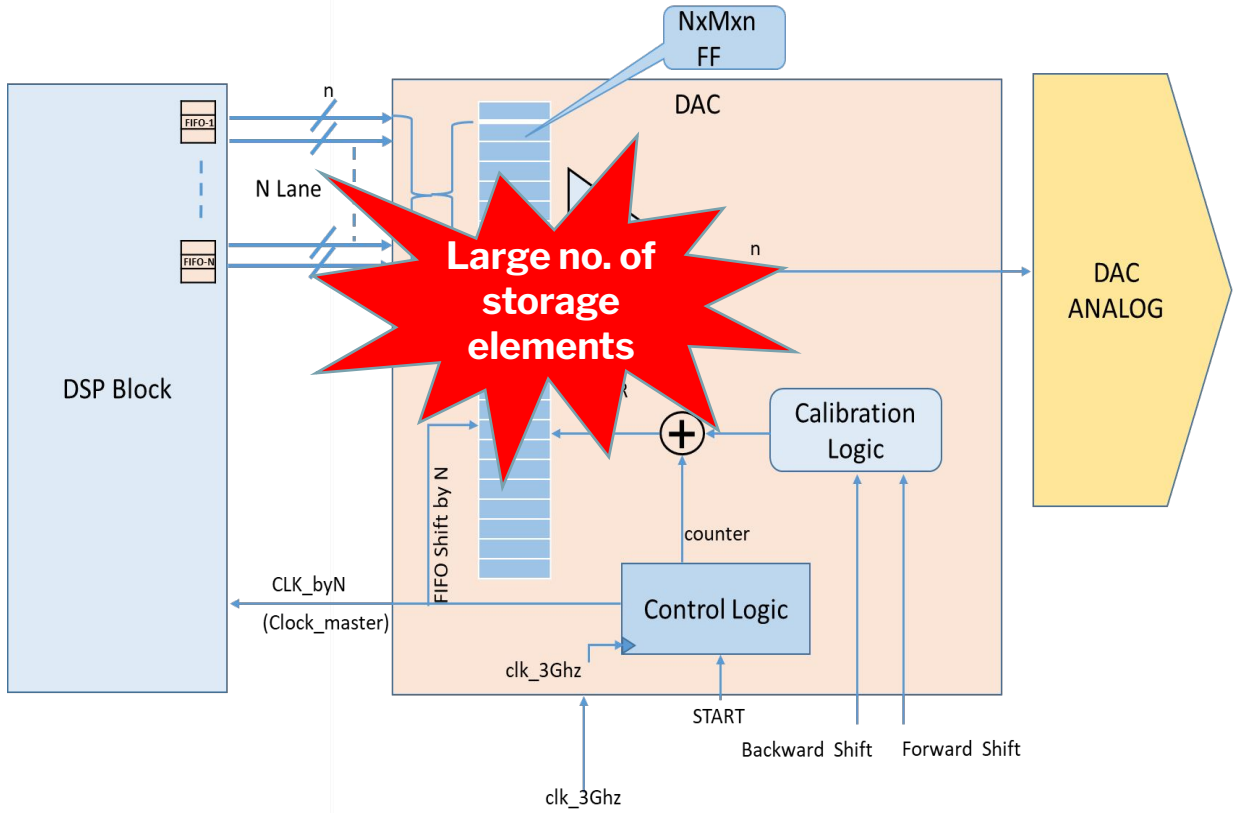
Contemporary solution

Store the data and adjust the read pointer to perform the group delay calibration and phase alignment

Using multiple high frequency pipelines to perform group delay calibration and phase alignment



Contemporary solution

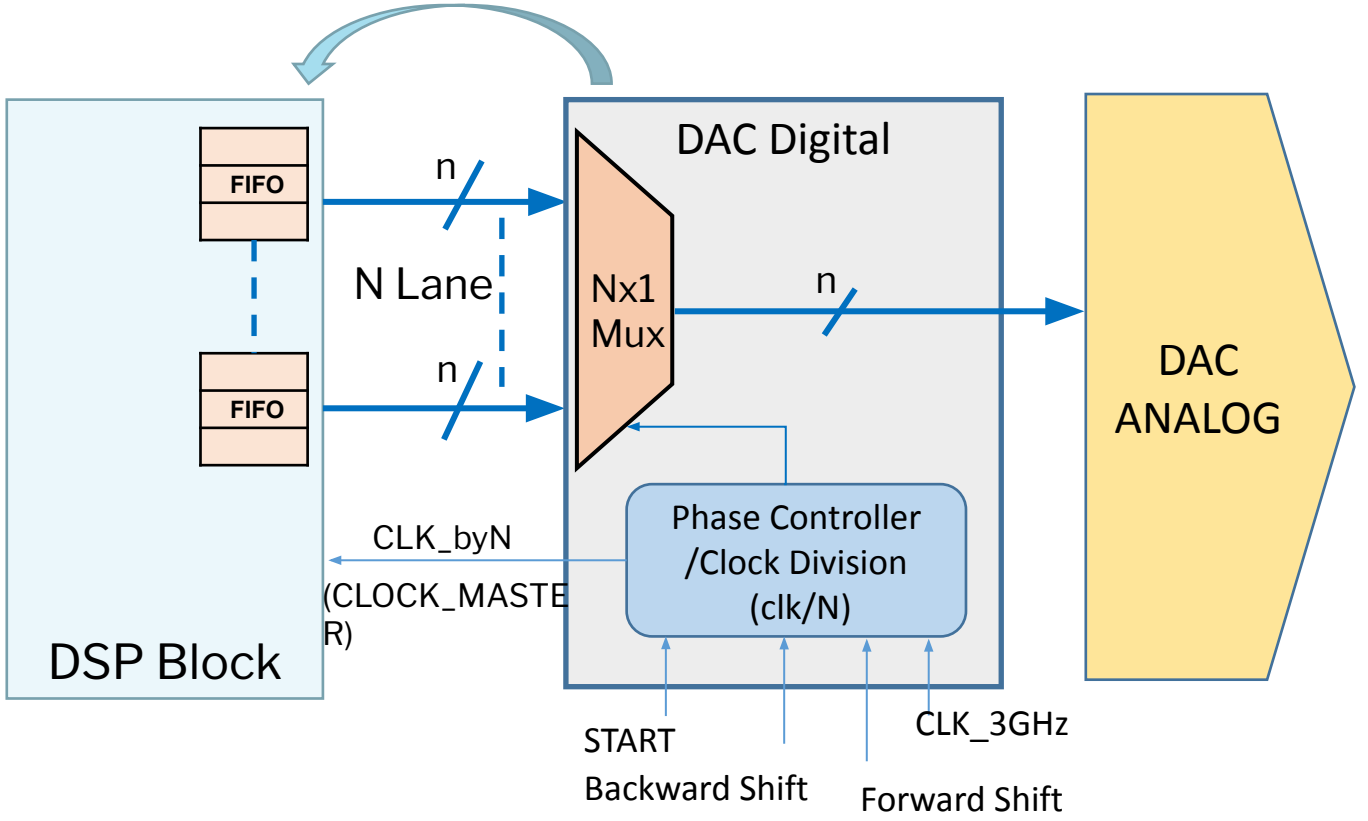


Drawbacks

- Large No. of Flip-Flop (NxMxN) needed to store the data
- Large number of FFs, so large area of structure
- Limited group delay option, depending on data storage
- High power consumption
- High implementation complexity for high-speed design

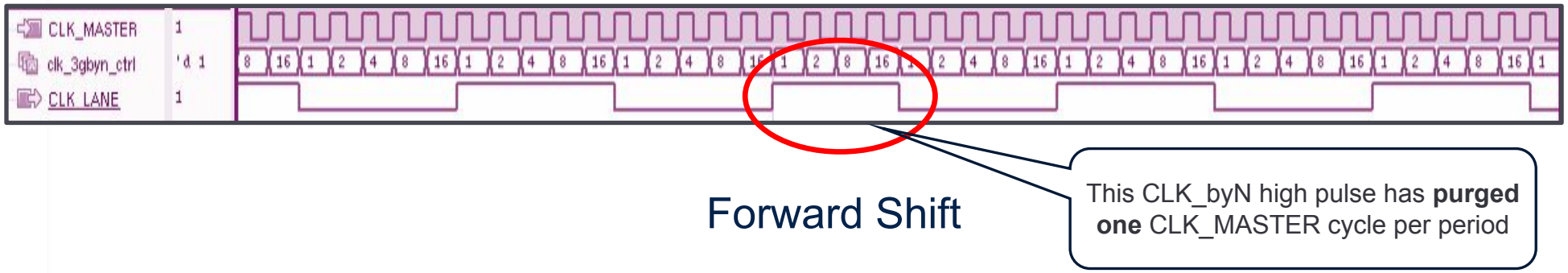
Main idea

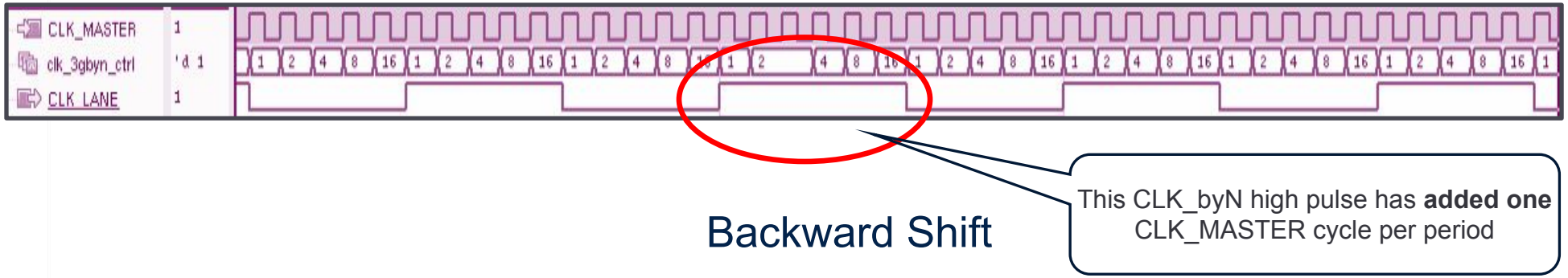
- Push the problem “**out of the box**”
- The FIFO in the DSP block repurposed as a delay modulator
- Master clock used to read the data from DSP clock
- Modulate the Master Clock from the DAC to the FIFO in the DSP block



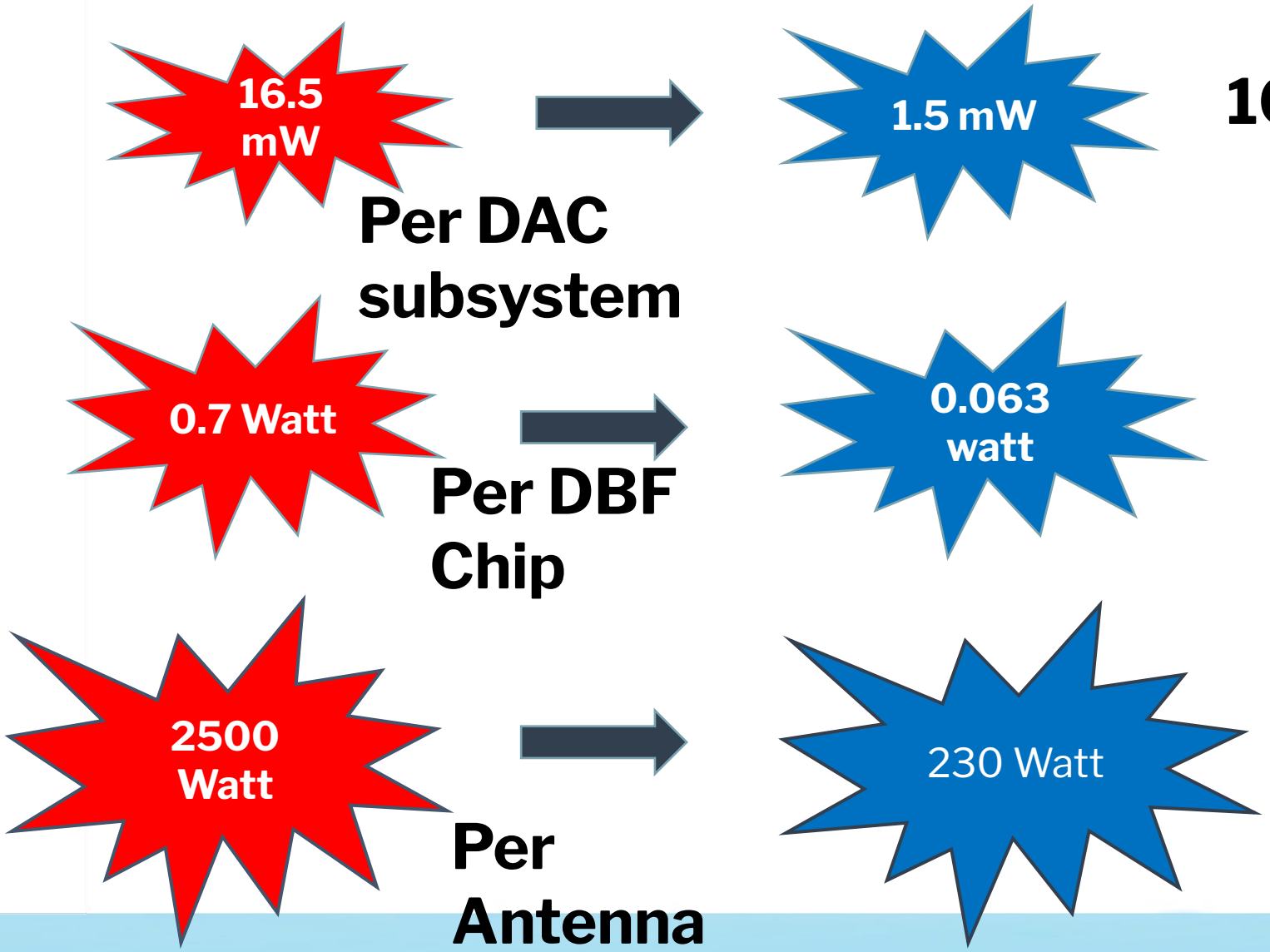
Main idea

- Modulate the Master Clock from the DAC to the FIFO in the DSP block
- Stretching and compressing the Master Clock will delay or advance the data stream coming to the DAC





Results



10X Power Reduction

4.5x area reduction

Summary

- The innovative design can accommodate **infinite time shift**
- The innovative architecture is scalable **without any extra storage overheads**
- **10x power & 4.5x area reduction** of DAC subsystem achieved
- **16% power saving** in total chip power
- The proposed architecture **simplifies the method**

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Thank You